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Abstract
Drain leakage current is a big problem for scaling the MOSFET's into the deep sub-micrometer regime. When the application voltages much lower than the breakdown voltage, a significant drain leakage current can be detected, with regards this current in scaled down complimentary metal-oxide-semiconductor (CMOS) devices for DRAM and/or EEPROM applications, and identified as the dominant leakage mechanism in discharging the DRAM storage node.
Generally, the drain leakage current impute to the carrier tunneling phenomena. The tunneling phenomena are high electric field effect. In the presence of a high electric field, carriers gain energy from the field as they drift along.
In modern VLSI devices, band to band tunneling has leaded to the significant leakage than cause the device performance less than anticipate and that is becoming one of the most important leakage current components. How to suppress the band to band tunneling is a strict challenge. Therefore, it is very important to have understanding and an accurate physical model to express the band to band tunneling current, particularly for applications such as the DRAM where leakage currents must be keep extremely low to lengthen the storage time.
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